PLL Frequency Synthesizers Based on the DDS in Feedback Loop

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This paper discusses the benefits and disadvantages of the one-loop PLL architecture based on the DDS in feedback loop. It presents mathematical model of phase noise sources with equations for its estimation while taking into account the performance of present-day components. The paper also presents spur-reducing approach based on the variable reference frequency. The equations for evaluating "bad" frequencies and spur offsets are given. As a measure of spur the empirical cumulative distribution of SFDR normalized to 1 GHz is used. It allows to evaluate and compare the quality of different synthesizers regardless of their frequency range. Synthesizers with single and dual frequency reference were compared using this measure. The paper also considers the locking process of the PLL based on the DDS in the loop.

Keywords—PLL; DDS; phase noise; spur; SFDR

I. INTRODUCTION

There are many papers and books about frequency synthesizers, their architectures and practical design, for example [1, 2]. But on the other hand, new components and their constantly increasing performance make the designers to look at old well known schemes with new angle. For example, modern direct digital synthesis (DDS) integrated circuits operating at more than 1 GHz clock frequency with 48-bit phase counter make it possible to use them as frequency dividers with extra fine resolution of dividing factor which can be varied in a wide range. This approach is mentioned in [3-5], so the idea of using the DDS in feedback loop of the PLL is not new, but there are not many papers which describe it in detail based on the real device measured data. Based on the experimental results, this paper tries to answer the following questions concerned the PLL with DDS in feedback loop:

- What the benefits of using DDS in feedback loop and what restrictions are imposed on the system components.

- What components are the bottleneck for phase noise performance in DDS based single loop PLL design and how it can be improved.

- How to compare the phase noise quality of different synthesizers.

- How to predict spurious frequencies and how to reduce spurs.

- How fast is the switching time of the DDS based PLL design.

- How to measure and compare spuriousness of different synthesizers.

II. ARCHITECTURE OVERVIEW

There are two approaches for fine resolution one-loop synthesizers. First one is based on the DDS at the reference input of the phase-frequency detector (PFD), figure 1, the second - on the DDS in the feedback loop, figure 2. Let's look at the first design in detail. The signal from low-frequency stable reference source (or external source) is fed to narrow band PLL that produces low phase noise, high frequency (about 1 GHz) reference signal that in turn is used as clock for DDS. The signal from DDS output is fed to low-pass filter and then to the reference input of PFD. Other parts of the PLL is quite standard, its feedback loop includes fixed high-frequency dividers which can be combined with N-integer dividers to reduce the output frequency range of DDS. This can eliminate some "bad" frequencies at its output.
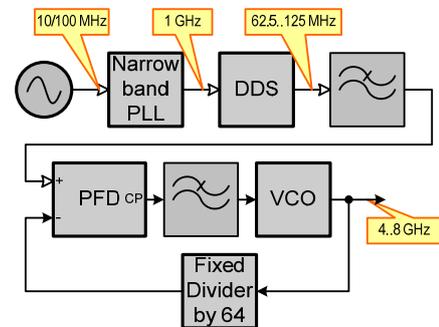

Figure 1. PLL based on the DDS in the reference path

The main benefit of the design, shown in figure 2, compared to the previously discussed, is that it doesn't require special high-frequency PLL for DDS clock, since it is produced by the VCO of main loop. There is no need in narrow-band high frequency and high cost SAW based VCO used in the first design. The approach, shown in figure 2, reduces size, cost and complexity of the synthesizer. The same way it can be used in multi-loop designs, where after frequency offset in the loop we can obtain signal in range 0.5 to 1 GHz, that can be used as a clock for DDS, see figure 3. It reduces the phase response gain in the main loop, and as a result, the output phase noise.
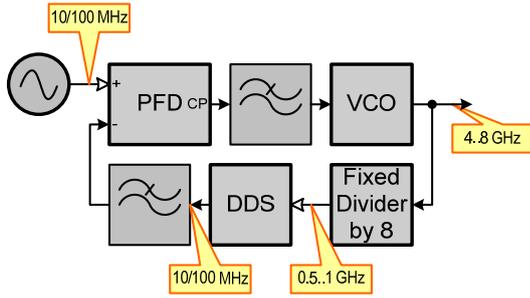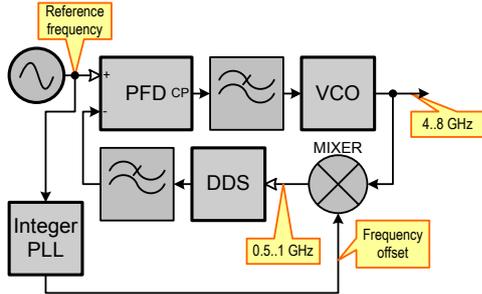
Figure 2.   PLL based on the DDS in feedback loop

Figure 3.   PLL with frequency offset in the loop

III.   SINGLE-LOOP DESIGN BASED ON THE DDS IN THE LOOP

A.   Operation Basics

Let's consider simple DDS based single-loop PLL, since the results can also be applied to a more complex cases. Figure 4 shows block diagram of Advantex LNO-HP34M-RF synthesizer.
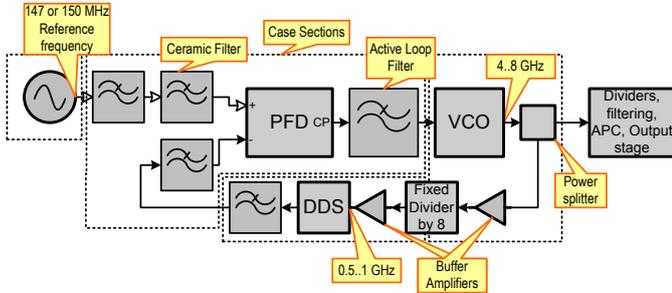

Figure 4.   Block diagram of Advantex LNO-HP34M-RF synthesizer

Reference frequency from internal TCXO or external source is applied to "+" input of the PFD. Its output is fed to the active loop filter, then to the VCO control input. RF signal from VCO is applied through power splitter to the output block (which includes dividers, harmonic filtering, automatic power control and power output stage) and to the loop, that consists of buffer amplifiers, fixed divider by 8, DDS and two low-pass filters. There are two filters for reference signal: one with 150 MHz pass-band based on discrete components, and second – 225 MHz low-pass ceramic filter located just near the "+" input of the PFD. The function of the first filter is to suppress possible interference signals in the middle band, while the second filter - to suppress RF signal induced on the reference lines input to PFD. It's very important part, in combination with

spatial isolation with aid of separate case sections, it defines the possible spur suppression. The buffer amplifiers in the loop, along with double filtering of DDS output, play the same role – to isolate PFD from VCO as far as possible.

The synthesizer is designed to operate with reference signals from 20 to 150 MHz. Actually to reduce output phase noise you need to retain the reference frequency high as possible (it will be discussed further in the paper). In this particular design it is limited by the DDS maximum clock rate. Output frequency (for DDS with 48-bit frequency tuning word and fixed divider by 8 for clock signal) is defined by the following equation:

$$f_{VCO} = f_{ref} \frac{2^{51}}{N_{FTW}},$$

(1)

where f_{VCO} – output frequency, f_{ref} – reference frequency, N_{FTW} – frequency tuning word value (integer). Output frequency step can be found from (1) as follows:

$$\frac{df_{VCO}}{dN_{FTW}} = -f_{ref} \frac{2^{51}}{N_{FTW}^2} =$$

$$= -\frac{f_{VCO}^2}{2^{51} f_{ref}}.$$

It's about 0.2 millihertz at 8 GHz output and 150 MHz reference.
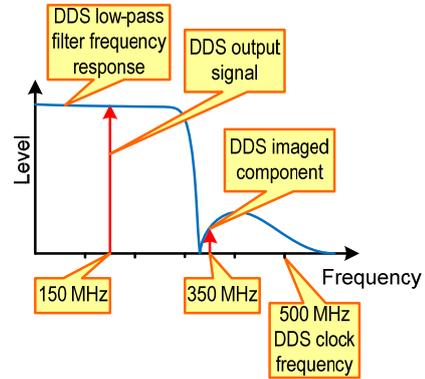

Figure 5.   DDS output spectrum at 4 GHz VCO

Let's consider the locking process of the system. At first suppose that PLL is locked at 4 GHz (VCO lower bound), and reference frequency is 150 MHz. DDS output frequency also equals to 150 MHz, since PLL is locked. DDS clock rate at this moment is $f_{VCO}/8$, i.e. 500 MHz. DDS output spectrum is shown in figure 5. From this figure it's clear that filter stopband should be not higher than 350 MHz, otherwise the imaged component of the signal is not suppressed. Then suppose that we want to switch the frequency of output signal from 4 to 8 GHz. To do it we need to load to DDS new FTW value that is

twice less than previous one. DDS output frequency is changed almost instantly unlike VCO frequency, which is relatively slow due to loop filter integrator. Just after the loading new FTW value, DDS output frequency will be 75 MHz, while f_{VCO} will stay at about 4 GHz for some time. PFD "sees" that frequency at "-" input (i.e. 75 MHz) is less than at "+" input (150 MHz) and tries to make f_{VCO} higher. After some time f_{VCO} settles to 8 GHz, DDS output frequency to 150 MHz, and PLL locks. DDS output spectrum when PLL is locked at 8 GHz is shown in figure 6.
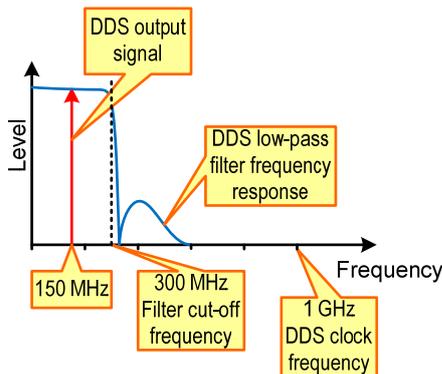

Figure 6.   DDS output spectrum at 8 GHz VCO

Consider the reverse process, i.e. switching from 8 to 4 GHz. To set new frequency we need to load new FTW value that is according to (1) twice greater than previous one. Just after the moment of loading DDS output frequency will be twice higher, i.e. 300 MHz, since FTW is already new, but f_{VCO} is still about 8 GHz. Thus DDS low-pass filter must have passband not less than 300 MHz, otherwise PFD will not "see" the signal at its "-" input, and PLL will not lock the frequency. In normal conditions PFD "sees" that frequency at "-" input (300 MHz) is higher than at "+" input (150 MHz) and tries to lower f_{VCO}, so after some time VCO settles to 4 GHz, and DDS output frequency – to 150 MHz accordingly.
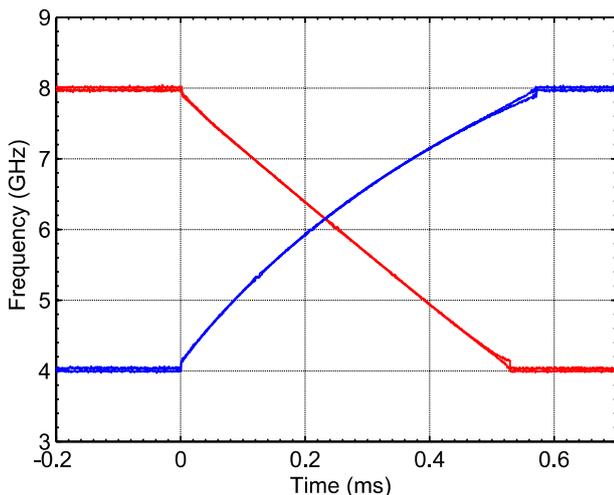

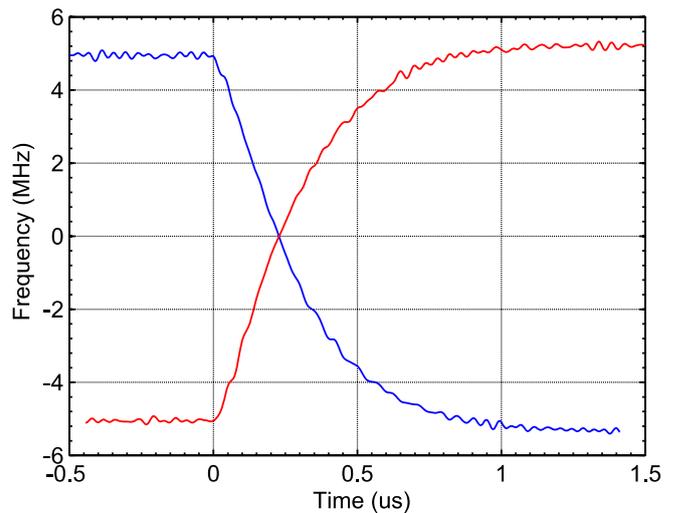Figure 7.   Frequency switching process for 4 to 8 GHz step

Figure 8.   Frequency switching for 10 MHz step at 6 GHz center frequency

Frequency switching process for LNO-HP34M-RF synthesizer is shown in figures 7 and 8. Switching from 4 to 8 GHz takes about 500 us in this example. Generally it depends on the loop filter bandwidth and its design [6]. But the primary goal of the loop filter is to provide stable locking process (i.e. enough phase margin) and low integral phase noise [1]. So in practice it's hard to improve switching time, while retaining optimum phase noise and stability. Another way to make switching process faster is to use special presetting scheme, see figure 9, where additional DAC signal is used to preset VCO control voltage at large frequency steps. It allows to eliminate the slow slew rate of the active loop filter integrator to some extent.
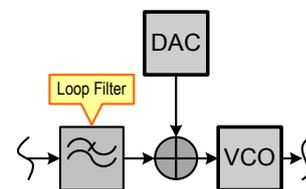

Figure 9.   VCO control signal presetting

From consideration of operation of the synthesizer based on the DDS in the loop we can conclude the following regarding the restrictions imposed on the system components:

- Fixed dividers before DDS should ensure proper DDS clock operation in all VCO operation range.

- PFD should have frequency range on "-" input as double the reference frequency on "+" input.

- DDS low-pass filter should have stopband frequency not higher than $f_{clk\ min}$-f_{ref}, where $f_{clk\ min}$ – minimum DDS clock frequency corresponding to VCO minimum frequency, while taking into account fixed dividers, f_{ref} – reference frequency at "+" input of the PFD.

- DDS low-pass filter should have passband frequency not less than twice of the reference frequency.

B. Phase Noise

When evaluating phase noise, sometimes it's more convenient to operate with normalized phase noise. It's also useful when comparing the quality of synthesizers with different frequencies. The idea of this method is the following.

Let's represent the original signal s(t) in the following form in time domain:

$$s(t) = e^{j(\omega_0 t + \varphi(t))},$$

where ω_0 – original signal frequency, $\varphi(t)$ – its phase noise at ω_0. Suppose that we have ideal frequency multiplier (or divider) with r factor, $r \in R$. It operates on the signal like power, i.e. as follows:

$$s(t)^r = e^{j(r\omega_0 t + r\varphi(t))}, \tag{2}$$

so we have new frequency equal to $r\omega_0$ and phase noise $r\varphi(t)$. Thus we found that phase noise is proportional to the frequency. It also means that spectral density of phase noise power is proportional frequency squared. Taking this in mind, we will use phase noise, normalized to some frequency, e.g. to 1 GHz, as follows:

$$\Phi_{1GHz} = 20\log(f) + \Phi_f, \tag{3}$$

where Φ_{1GHz} – phase noise in dBc/Hz normalized to 1 GHz, f – original frequency, expressed in GHz, Φ_f – absolute phase noise at frequency f. If phase noise of both sources is normalized, then it is possible to compare their quality.
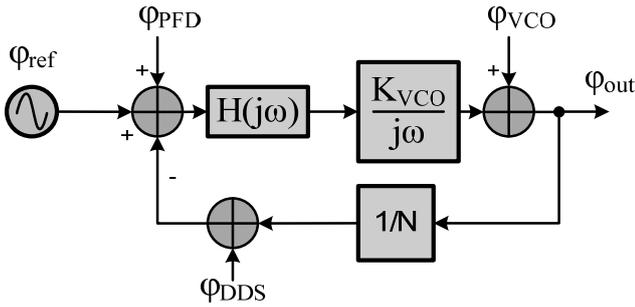
Figure 10. Simplified PLL model of phase noise sources

Figure 10 shows a simplified model of the PLL, presented in figure 2, with phase noise sources. Output phase noise according to this model is the following:

$$\varphi_{out} = \frac{NK_{VCO}H(j\omega)(\varphi_{ref} + \varphi_{PFD} - \varphi_{DDS})}{j\omega N + K_{VCO}H(j\omega)} +$$

$$+ \frac{\varphi_{VCO}}{1 + \frac{K_{VCO}H(j\omega)}{j\omega N}},$$

where φ_{out} – output phase noise, N – total loop division factor (including DDS and fixed dividers), K_{VCO} – VCO slope, $H(j\omega)$ – loop filter frequency response, φ_{ref} – phase noise of reference source, φ_{PFD} – PFD phase noise, φ_{DDS} – DDS phase noise, φ_{VCO} – VCO phase noise. For small frequency offset we can simplify the above equation, since $H(j\omega) \to \infty$ at $\omega \to 0$:

$$\lim_{\omega \to 0} \varphi_{out} = N(\varphi_{ref} + \varphi_{PFD} - \varphi_{DDS}).$$

Thus to evaluate the normalized phase noise at the PLL output at small frequency offset we need just to add normalized values from all sources except VCO (because its noise is suppressed by the loop filter at small offset). So we can easily evaluate the impact of each component. For PLL implemented in LNO-HP34M-RF synthesizer φ_{ref} is about −130 dBc/Hz, φ_{PFD} is about −129 dBc/Hz (including loop filter noise), φ_{DDS} is about −132 dBc/Hz (here are given the values normalized to 1 GHz). The values are almost equal, so in this case to reduce output phase noise we need to improve each component mentioned above. Actual phase noise of given synthesizer is shown in figure 11.
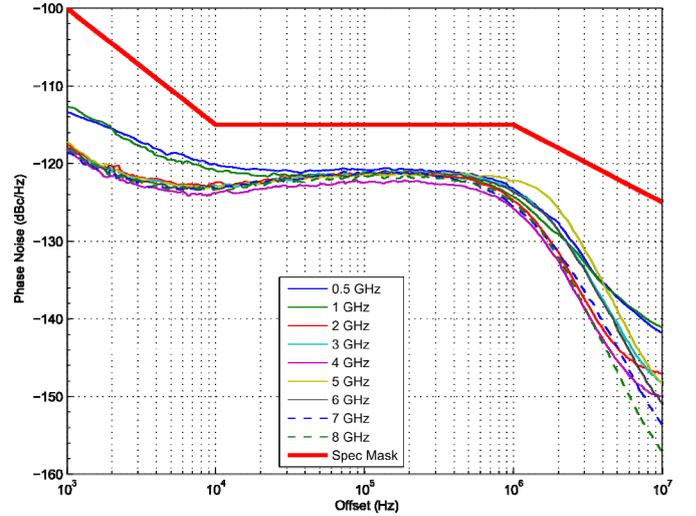
Figure 11. Phase noise of LNO-HP34M-RF synthesizer normalized to 1 GHz

PFD phase noise can be reduced by raising the reference frequency. If we make 600 MHz reference, it will gain 6 dB against actual at 150 MHz. One of the best phase-frequency detectors, HMC439QS16G (Hittite), can operate at up to 1.3 GHz and has noise floor (normalized to 1 GHz) about −140 dBc/Hz at 10 kHz offset at 600 MHz reference. Modern 3.5 GSPS DDS, AD9914 (Analog Devices) has normalized to 1 GHz phase noise about −139 dBc/Hz. So these components theoretically make it possible to achieve output phase noise about −136 dBc/Hz at 10 kHz offset at 1 GHz using single-loop architecture described above.

It worth to note that reference frequency should be high enough, since normalized PFD phase noise performance rises with operating frequency. That's why fast clock rate DDS is so important. The second reason of using high reference frequency in the design is that it's very hard to work with low-frequency signals while retaining their phase noise quality, since it imposes strong requirements on power supply system and amplifiers. For example, −140 dBc/Hz 1 GHz signal corresponds to −180 dBc/Hz 10 MHz signal. For 0 dBm 10 MHz signal such quality is unreal, since thermal noise is about −174 dBm/Hz.

C. Spurs

One of the most problems of single-loop design – it's the spurs generated by DDS and VCO signal induced on the PFD inputs. Since the phase gain is quite high (f_{VCO}/f_{ref}), even low spurs at the DDS output may result in a very spurious VCO output signal.

The main spur sources are the following:

- Spurs at "-" input of PFD generated by the DDS itself.

- Spurs generated by VCO signal induced on PFD inputs.

- Sur generated by PFD at reference frequency offset due to charge-pump or loop filter leakages.

- Spurs due to reference frequency induced on VCO.

Last three cases can be resolved by high isolation of PFD, inserting ceramic filters on its inputs, and adding buffer isolation amplifiers before loop dividers. The first one can be partially resolved with aid of spur killers built in DDS, but this method is limited to the number of spurs that can be suppressed (2 or less in most cases), and to its order. And not all DDS have spur killer.

The spurs for the design shown in figure 2 can be expressed by the following equation:

$$\pm m f_{ref} \mp n \frac{f_{VCO}}{8} = \Delta f,$$

(4)

where m and n – integer numbers which define the spur order, f_{ref} – reference frequency (DDS output frequency), f_{VCO} – VCO frequency ($f_{VCO}/8$ – DDS clock frequency), Δf – spur offset from VCO frequency f_{VCO}. At high Δf, i.e. greater than loop filter bandwidth, the spurs are suppressed by the loop filter according to its frequency response figure. Thus the largest spurs are encountered within narrow band offset, typically less than 1 MHz from center frequency. It also should be noted that spurs of the signal fed to some divider or multiplier remain at the same offsets, but its level is changed as shown in (2). For this reason it's convenient to use normalized values (e.g. to 1 GHz) like we do for phase noise (3). Further in the paper we will use SFDR term (spurious free dynamic range) expressed in dBc. It's the difference of levels between fundamental signal and maximum spur within the defined maximum offset from the carrier. So it's a good practice to

specify SFDR with the band and center frequency values, e.g. SFDR is 90 dBc in 1 MHz band at 1 GHz. In this paper we will treat SFDR as a positive number, i.e. the greater SFDR – the lower spurs. Generally the higher the spur order (i.e. m and n values in (4)), the better SFDR (i.e. lower spur levels), but sometimes spurs with greater order have higher level. It depends on the impact of each spur source on the final result in a particular design.

Let's evaluate SFDR at VCO output. Typical narrow-band SFDR performance of 14-bit DDS for 150 MHz output and 1 GHz clock rate is about 86 dBc. Phase gain at 8 GHz VCO output is 20log(8000/150)≈34.5 dB, so SFDR at the VCO output will be 86 − 34.5 = 51.5 dBc. It also should be noted that DDS low-order spurs (i.e. when output to clock rate ratio is about 1⁄3, 1⁄4, 2⁄5 etc.) are not specified in most cases, since SFDR near these ratios can be really bad.

So there are two ways to improve SFDR. First and straight method is to reduce phase gain using frequency offset in the loop as shown in figure 3. It's a common approach used in multi-loop designs that reduces not only spurs but phase noise as well. The main problem is the complexity of the design.
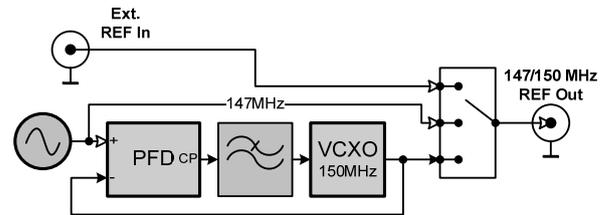

Figure 12. Block diagram of spur redusing option (HPSS) implemented in Advantex SG8 signal generator

Another way to improve SFDR is to avoid low-order spurs by selecting multiple reference frequencies, when "bad" output frequencies for one reference are covered by "good" ones for another. From (4) it's clear that these reference frequencies should form high order ratios, e.g. like 50/49 or 51/50 etc.) and should have small frequency difference, otherwise "good" and "bad" frequency bands will be too far shifted, and will not cover each other. Figure 12 shows the block diagram of HPSS spur reducing option for Advantex SG8 signal generator based on the LNO-HP34M-RF synthesizer. The 150 MHz reference is produced from 147 MHz TCXO by narrow-band PLL using the VCXO with low phase noise. This allows to make 150 MHz source strongly phase aligned to 147 MHz reference with 50/49 ratio.

Synthesizers may have different frequency ranges and various designs, so to compare its spur performance we need at least to define the following:

- Reliable measurement technique which is not limited to any particular design, and converges to the same results at different measurement conditions, i.e. it shouldn't miss the spurious frequencies.

- Some integral measure of synthesizer SFDR quality, that as far as possible doesn't depend on particular frequency range of the synthesizer. The simple spur graph is not informative since many vertical lines with

totally different height concentrated near each point of X axis make it impossible to compare the graphs.

D. On the SFDR Measurement Technique

As a rule SFDR measurement is a time consuming procedure especially for wide-band synthesizers. And potentially, more time you spend (less frequency step – more points), more reliable results you get. At first, let's define the following terms of measurement:

- frequency range of output signal;

- SFDR band, i.e. maximum frequency offset from center frequency, where spurs to be measured;

- frequency grid (center frequencies).

If synthesizer uses dividers after octave VCO to implement extended frequency range, in most cases it will be enough to limit the total range to one upper octave, since normalized SFDR will have the same values at lower bands.

It's better for the SFDR band to be not less than PLL passband, since the spurs are not suppressed here by the loop filter.

The step of the frequency grid should be much less than SFDR band. It's important for reliable measurements, since the frequency offset of high order spurs is proportional to the change of center frequency with factor which can be greater than one. So if the step is too great we can miss the spurs, since they may appear to be far out of the PLL passband for given center frequency. On the other hand it can take too long time for such small frequency steps, so we need to find some solution to avoid this problem. In most cases the reference frequencies are multiple to 1 MHz, so if we take the step equal to 1 MHz but with some small offset, e.g. about 100 kHz (forming the grid like 1000.1, 1001.1, 1002.1,.. MHz), we will not miss even high order spurs despite the relatively large center frequency step.

The time spent for measurement also depends on the SFDR limit to be used, which in turn depends on the RBW set to spectrum analyzer.

E. On the Measure of Synthesizer Spuriousness

As a measure of synthesizer spuriousness the empirical cdf (cumulative distribution function) of normalized SFDR can be used. Suppose that we have reliable (i.e. without missed spurs) results for all given band taken with defined step. First we need to normalize these values to some frequency, e.g. to 1 GHz:

$$SFDRN_i = SFDR_i + 20 \log f_i, \tag{5}$$

where $SFDRN_i$ – normalized SFDR in dBc, $SFDR_i$ – measured data (in dBc) at center frequency f_i expressed in GHz. Empirical cdf (ECDF) of normalized SFDR (SFDRN) can be expressed as follows:

$$ECDF(SFDRN) = \frac{1}{N} \sum_{i=1}^{N} 1\{SFDRN_i \le SFDRN\},$$

where N – total number of center frequencies. Thus we have a graph that on Y axis represents the evaluated probability to encounter spur with normalized SFDR less than given at X axis. Since the distribution of spurs in most cases is near to uniform, this probability will be about the same for all center frequencies within total band.
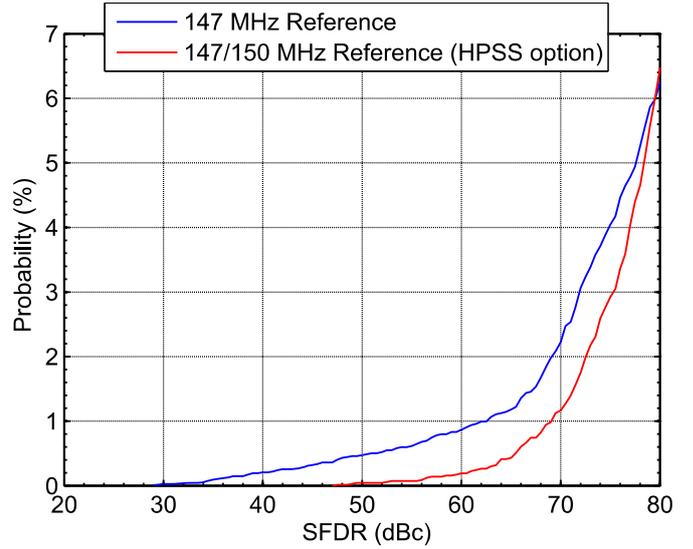

Figure 13. Empirical cdf of 1MHz BW SFDR normalized to 1 GHz for LNO-HP34M-RF synthesizer alone and with HPSS spur reducing option

Figure 13 shows empirical cdf for normalized SFDR of LNO-HP34M-RF synthesizer with 147 MHz single reference, and in combination with HPSS spur suppression option based on 147/150 MHz switching reference. SFDR bandwidth is 1 MHz for both cases, the measurements were made in 4 to 8 GHz band with 1 MHz step with 100 kHz offset.

Let's consider how to use this graph by the following example. Suppose that we have 1000 frequency points distributed near 2 GHz. And we need to know how many frequencies we encounter with spurs worse than 60 dBc.

According to (5) 60 dBc SFDR at 2 GHz correspond to 66 dBc of normalized SFDR. From the figure we find that probability to encounter the frequency with SFDRN less than 66 dBc is about 1.4% for synthesizer alone, and 0.6% with HPSS option. It means that from 1000 points we encounter 14 and 6 points with absolute SFDR worse than 60 dBc for synthesizer alone and with HPSS option respectively.

IV. CONCLUSION

In this paper we discussed the operation of PLL based on the DDS in feedback loop. Its benefits and disadvantages, phase noise and spurs were considered. Special attention was paid to SFDR measurement and representation of the results.

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