Frequency Synthesizer

DSG-3xM

Datasheet

Rev. 1.0

Advantex LLC

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Russian Federation, 111250, Moscow,
Krasnokazarmennaya st., 13/1
tel. +7 (495) 721-47-74, +7(495) 728-08-03
info@advantex.ru
http://advantex-rf.com, www.advantex.ru

IF/RF & Microwave Design
AdvanteX

Document Revisions

Rev.	Date	Description
1.0	June 06, 2014	DSG-3xM Frequency Synthesizer Datasheet (starting from DSG-03M-RF)

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1 Overview

1.1 Applications

- Arbitrary reference frequency source for one-loop PLL systems for spur suppression
- Coherent reference sources

1.2 Features

Short-form specifications are given below. Detailed data and additional conditions for these values are given in section 3 on page 8.

- Output frequency range: **0.5–250 MHz**
- Frequency resolution: **3.5 μHz**
- Spectral purity
  - phase noise: **−145 dBc/Hz** @ 10kHz offset @ 100 MHz
  - non-harmonics (±250kHz offset): **−95 dBc**
  - harmonics: **−50 dBc** @ 0 dBm
- Output level:
  - range **0 to +10 dBm** (RF Out3) and **+3 to +13** dBm (RF Out1 and RF Out2)
  - step **0.02 dB**
  - flatness (uncalibrated): **±2.5 dB**
- Phase shift control:
  - adjusting range: **0 to 360º**
  - min step: **0.022º**
- External reference input: **1 to 250 MHz** with 1 MHz step
- Reference output: **10 MHz**
- Programming interface: **SPI**

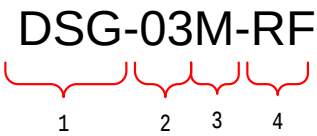

Figure 1: Module part number

Table 1: Part number fields description

Marking	Description
Field 1. Instrument series	
DSG	**D**irect Digital **S**ignal **G**enerator
Field 2. Revision	
03	Instrument revision number①
Field 3. Software options and assembly variants②	
M	Internal reference frequency source 10 MHz③
Field 4. Case type④	
RF	Milled aluminum alloy case (“RF”), “PCB” – w/o case (only PCB)

① Instrument revision number is changed when significant modifications concerned the functional characteristics of the instrument were made
② PCB assembly variant and CPLD firmware revision
③ Default assembly and firmware variant
④ Ordering without case is available on demand (i.e. as a PCB board)

1.3 Part Numbering

The module part number consists of the following fields (fig. 1):

1. Instrument series (project name)
2. Revision
3. Assembly variant
4. Case (body) type

Table contains the detailed description of the part number fields and auxiliary options. They appear in part number in the same order as listed in the table 1.

2 General Description

2.1 Block Diagram

Figure 2 shows the block diagram of DSG synthesizer. It features an integrated narrow-band N-integer phase-locked loop (PLL) system that allows reference

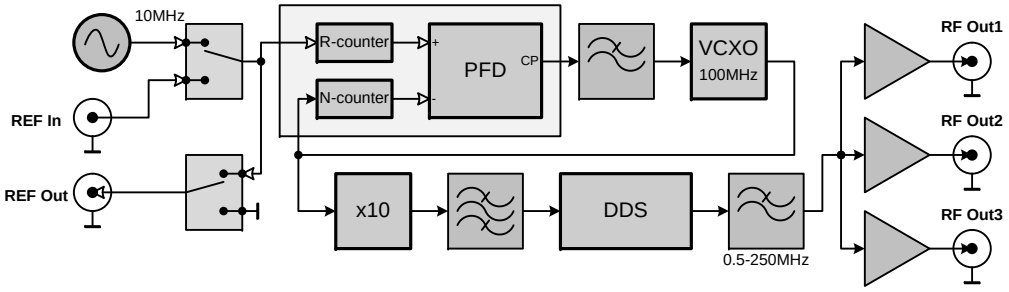

Figure 2: Block diagram of DSG synthesizer module

frequency inputs in range 1 to 250 MHz with 1 MHz step. PLL system generates 100 MHz low-phase noise signal followed by x10 frequency multiplier for 1 GHz clock signal used in direct digital synthesizer (DDS). Embedded DDS has 48-bit frequency tuning word, 14-bit phase tuning word (PTW) and 14-bit digital-to-analog converter (DAC). DSG synthesizer has three buffered outputs for easy signal distribution with levels up to +10 dBm (RF Out1 and RF Out 2) and up to +13 dBm (RF Out3).

Frequency step is defined by the following equation

$$\Delta f[Hz] = \frac{10^9}{2^{48}}.$$

Phase shift step

$$\Delta\varphi[rad] = \frac{2\pi}{2^{14}}.$$

2.2 Interfaces and Connectors

Synthesizer can be supplied with heatsink for better power dissipation (see HS-LNO option).

Figures 3, 4, 5 show external interfaces and connectors of DSG-3xM-RF synthesizer. The module has the following connectors:

RF Out1, RF Out2, RF Out3 – RF signal outputs, 0.5 MHz to 250 MHz frequency range with about $3.5 \cdot 10^{-6}$ Hz step, 0 to +10 dBm level range (RF Out1 and RF Out2), +3 to +13 dBm level range (RF Out3) with about 0.02 dB step, connector type – SMA, female;

REF In – input of optional external reference frequency signal, rated level 0 dBm. Signal of any frequency multiple to 1 MHz can be applied in 1 to 250 MHz range;

REF Out – output of reference frequency signal that is in use at the moment, output level about +10 dBm. If external signal is used as the reference (applied to REF In) then REF Out duplicates this signal, if internal TCXO is used, it duplicates internal reference signal (10 MHz);

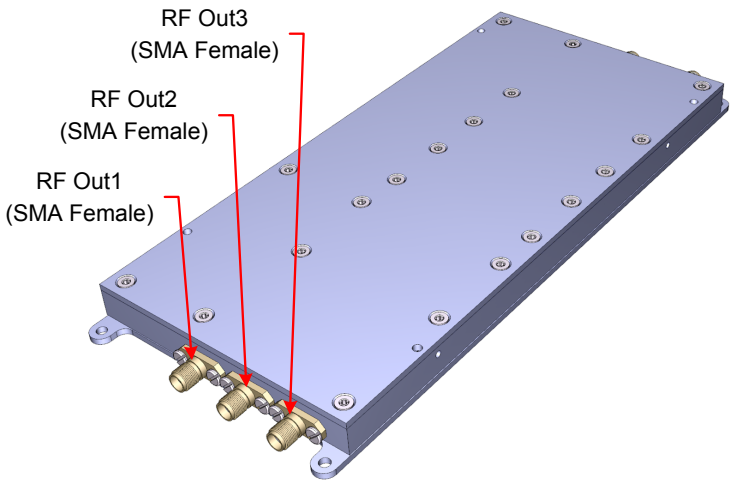

Figure 3: RF Out Connectors

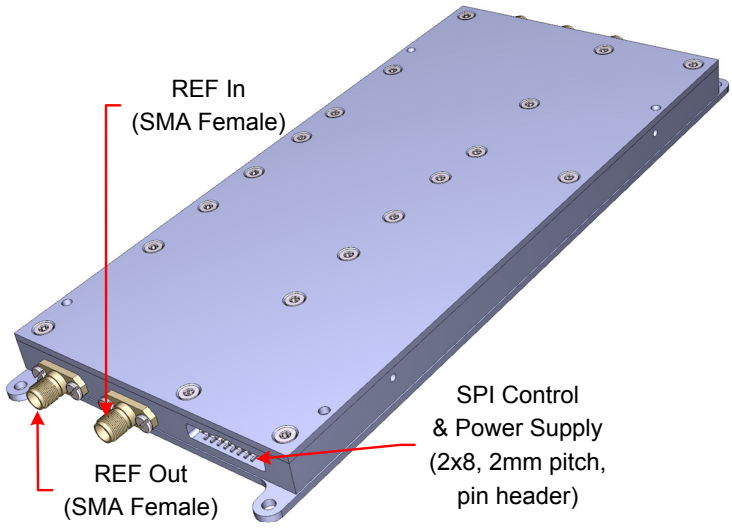

Figure 4: REF In, REF Out and SPI Connectors

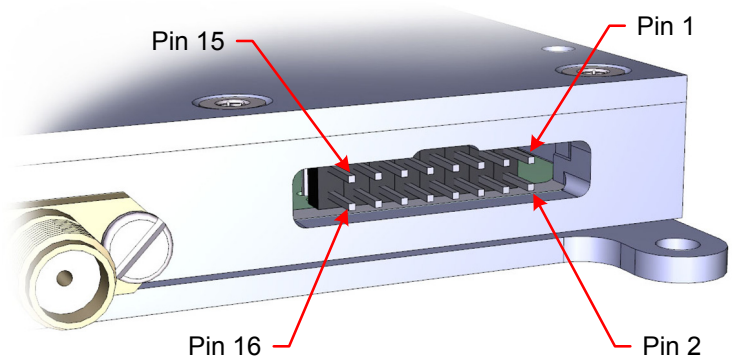

Figure 5: SPI Control and Power Supply interface

SPI Control and Power Supply – SPI interface designed to control DSG module, LVTTL 3.3V levels, max. clock rate is 20 MHz (except FLASH and Temperature Sensor operations – 10 MHz). Connector type: 2 row, 2 mm pitch, 16-pin holder.

Table 2 shows pinout of SPI Control and Power Supply interface.

3 Specification

Tables 3 and 4 shows specifications of DSG synthesizer, figures 6, 7 – absolute SSB phase noise, figures 8, 9 – phase noise normalized to 1 GHz according equation $\Phi_{1GHz}[dBc/Hz] = \Phi_{fc} + 20\log(1GHz/f_c)$. Normalized phase noise figures help to compare signal quality at different center frequencies f_c. Frequency response for maximum and minimum output levels is shown on figure 10. 2-nd and 3-rd harmonic levels (referred to fundamental harmonic) are shown on figures 11, 12.

Table 2: SPI Control and Power Supply pinout

Pin #	Name	Direction (relative to module)	Description (CTL_SPI bus signals)
1	MOSI	In	SPI master output, slave input
3	SS#	In	SPI select signal, data are latched only if this signal is active (“0” state)
5	SCK	In	SPI clock signal, data are latched by rising edge of SCK signal
7	MISO	Out	SPI master input, slave output
8	AUX	Out	Buffered PLL (ADF4002) MUXOUT signal. Can be used as Interrupt signal: “0” – normal condition, “1” – PLL NOT LOCKED condition. For more details see DSG Programming Manual. AUX pin is connected to CPLD via 1 kOhm resistor, so if not used you can tie it to GND
2, 10, 12, 14, 16	GND	–	Ground pins, internally connected to the case body
4, 6	–	In	Not used, can be left unconnected or tied to ground
9, 11	+5V	In	Positive power supply, +5.0 to +5.5V allowed. Rated current 190mA
13, 15	+9V	In	Positive power supply, +9 to +12V allowed, but to reduce overheating and power consumption it’s better not to exceed +10V. Rated current 480mA

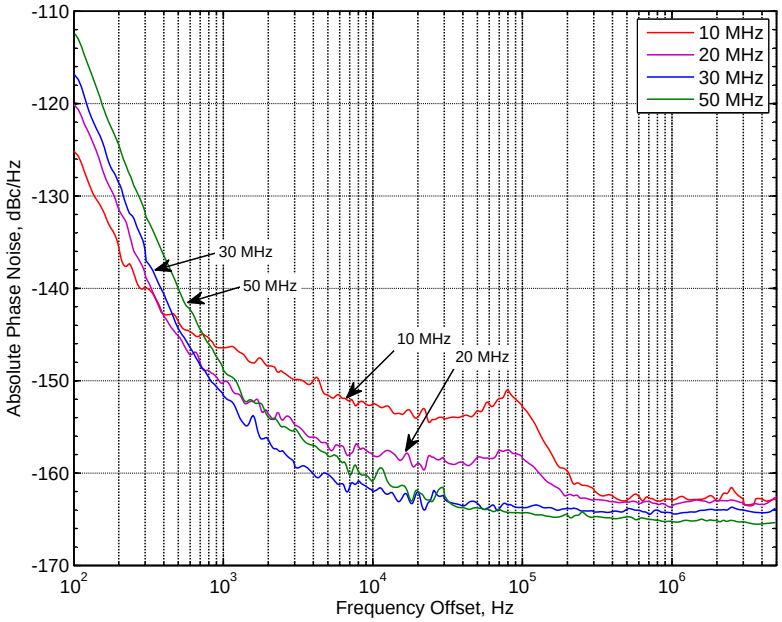

Figure 6: SSB phase noise at 10, 20, 30 and 50 MHz

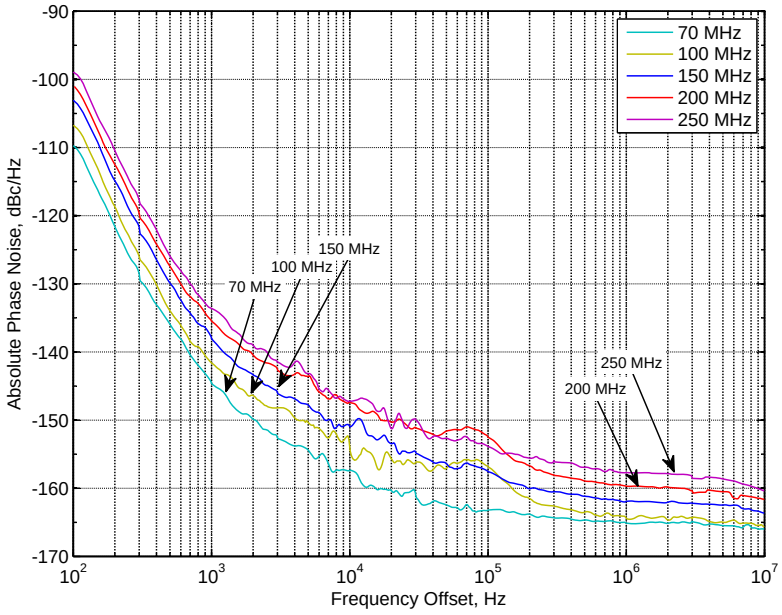

Figure 7: SSB phase noise at 70, 100, 150, 200 and 250 MHz

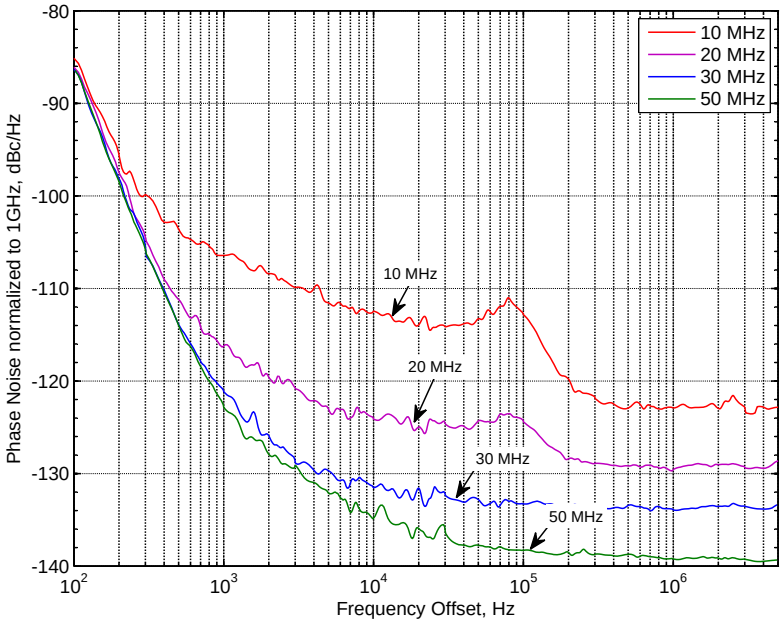

Figure 8: Phase noise normalized to 1GHz at 10, 20, 30 and 50 MHz center frequencies

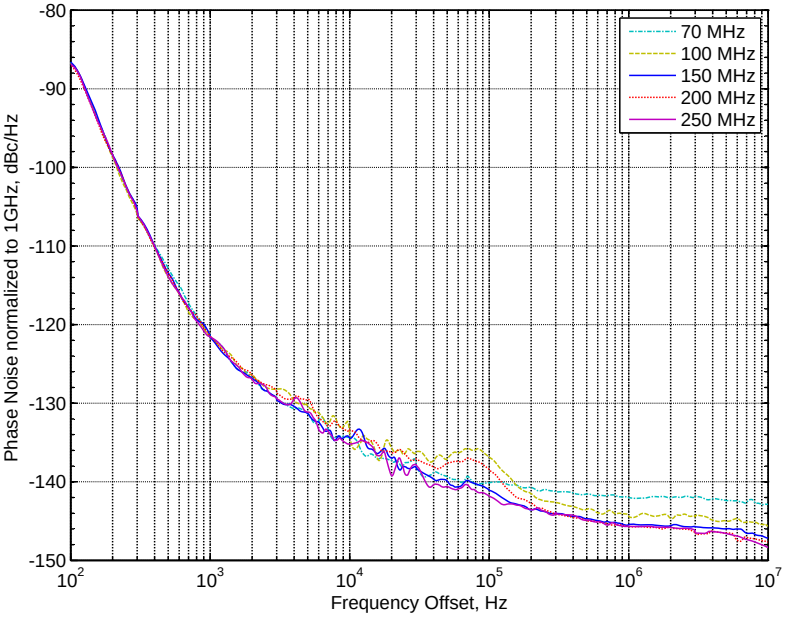

Figure 9: Phase noise normalized to 1GHz at 70, 100, 150, 200 and 250 MHz center frequencies

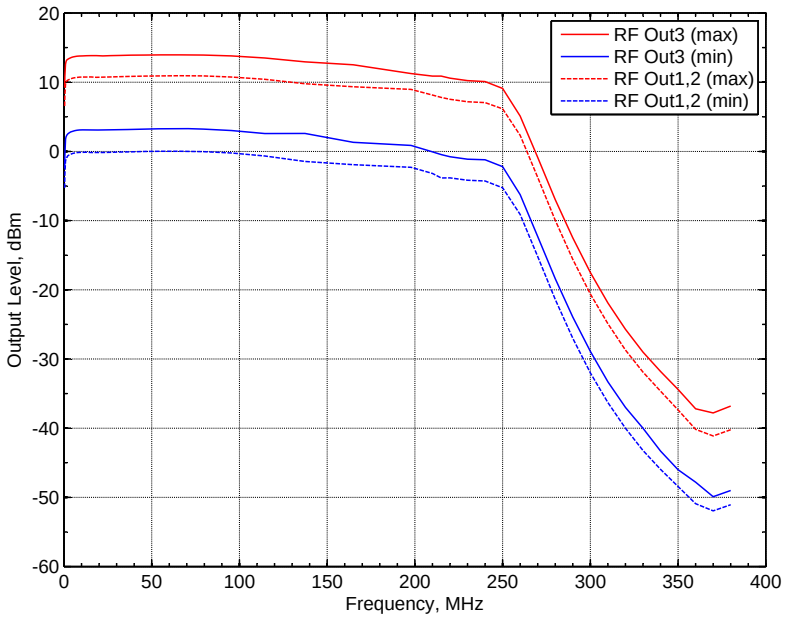

Figure 10: Frequency response of RF Out1,2,3 outputs at maximum and minimum levels

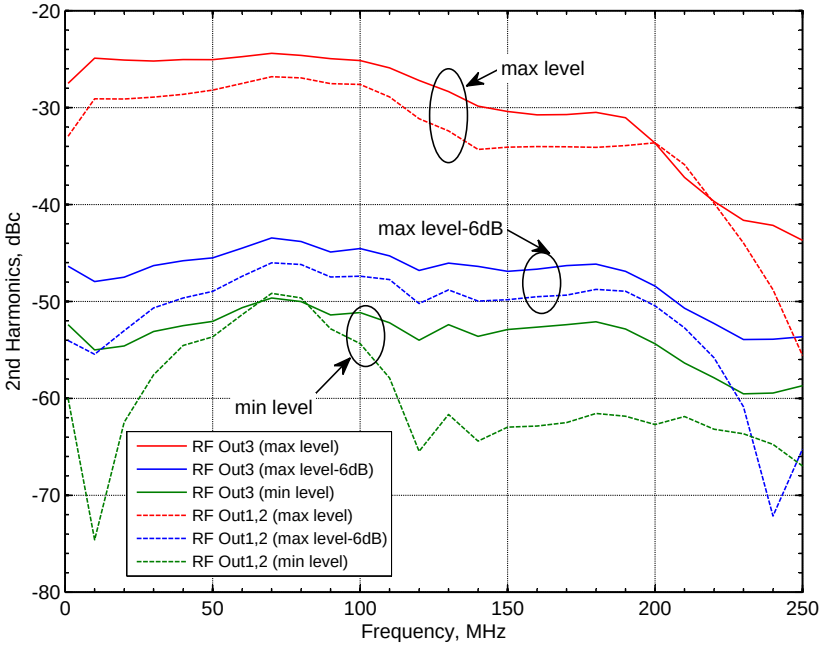

Figure 11: 2-nd harmonics levels

Table 3: DSG signal characteristics

Parameter	Conditions	min	max	Unit
RF Output				
Frequency range		0.5	250	MHz
Frequency step		3.5		μHz
Phase adjustment		0	360	degree
Phase step		0.022		degree
Output level	RF Out1,2 @ 100 MHz @ 50Ω load	0	+10	dBm
	RF Out3 @ 100 MHz @ 50Ω load	+3	+13	dBm
Level step		0.02		dB
Level accuracy	relative min level	±0.2		dB
Level flatness	within all frequency range	±2.5		dB
VSWR	RF Out1 and RF Out2 @ 50Ω load		1.2	
	RF Out3 @ 50Ω load		1.8	
Spectral purity				
Phase noise @ 100 MHz	100 Hz offset	−107		dBc/Hz
	1 kHz offset	−142		
	10 kHz offset	−155		
	100 kHz offset	−157		
	1 MHz offset	−165		
	10 MHz offset	−166		
2-nd harmonics	within all frequency range at max. output level - 6dB		−42	dBc
3-rd harmonics	within all frequency range at max. output level - 6dB		−45	dBc
Non-harmonics	within ±250kHz offset		−91	dBc
Internal reference				
Frequency		10		MHz
Temperature stability	Internal 0..+70°C	±3		ppm
	Internal −40..+80°C	±5		ppm
Aging	1st year	±1		ppm
REF Out level	Internal TCXO is ON	+9.5		dBm
Gain	External REF In (REF Out P1dB=+12dBm), 50Ω load	+10		dB
External reference input (REF In)				
Input frequency	with 1 MHz step	1	250	MHz
Input level	50Ω load	−10	+10	dBm
Stability		±20		ppm

Table 4: DSG Power supply and SPI

Parameter	Conditions	min	max	Unit
SPI Interface				
V_{IL}		−0.3	0.8	V
V_{IH}		2.0	3.9	V
V_{OL}	I_{OL}=0.1 (8) mA	0	0.2 (0.4)	V
V_{OH}	I_{OL}=0.1 (8) mA	3.1 (2.9)	3.3	V
CLK frequency	except Temperature sensor and FLASH operations		20	MHz
	all operations		10	MHz
Power consumption				
+5V		+5	+5.5	Vdc
+9V		+9	+12	Vdc
Stand-by mode current	+5V		9	mA
	+9V		10	mA
Normal mode current (RF Outputs are ON)	+5V		190	mA
	+9V		480	mA
Operating temperature		−40	+65	ºC
Dimensions	length w/o SMA connectors	185		mm
	width	87.5		mm
	height	13		mm
Weight		0.36		kg

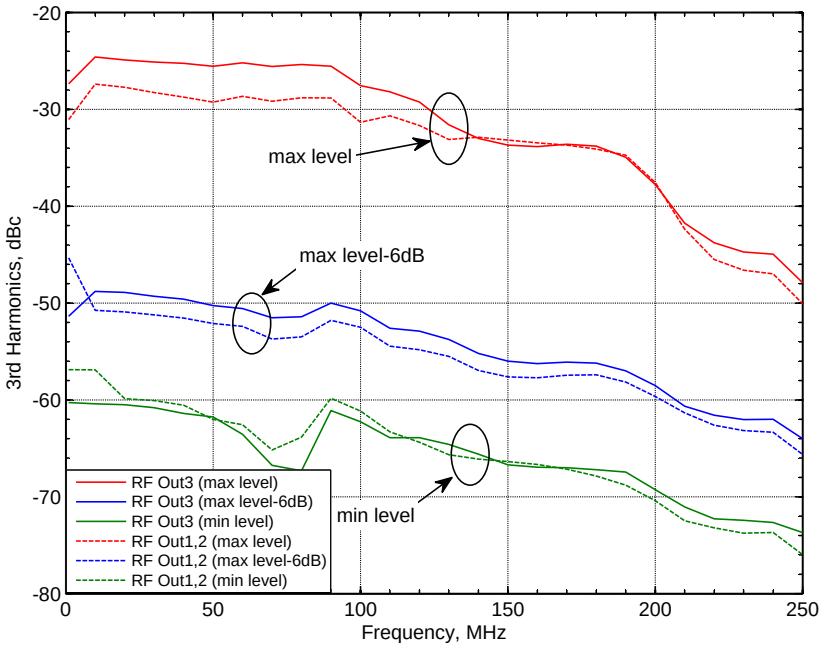

Figure 12: 3-rd harmonics levels