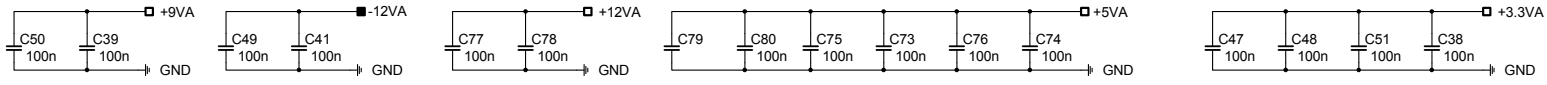
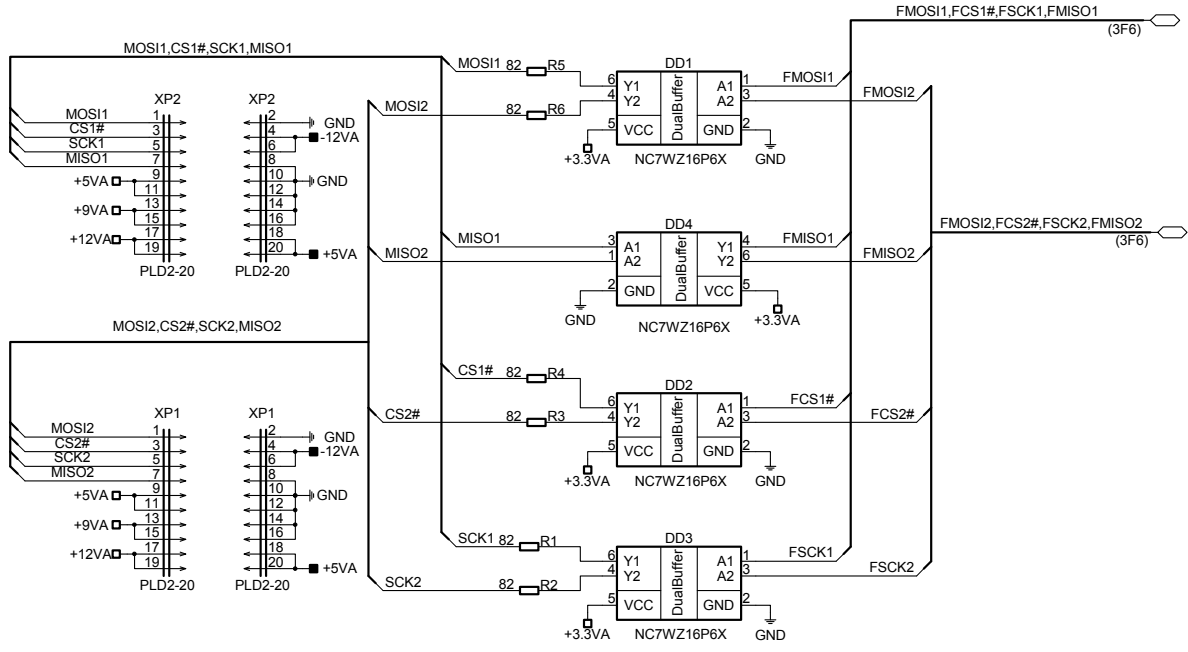
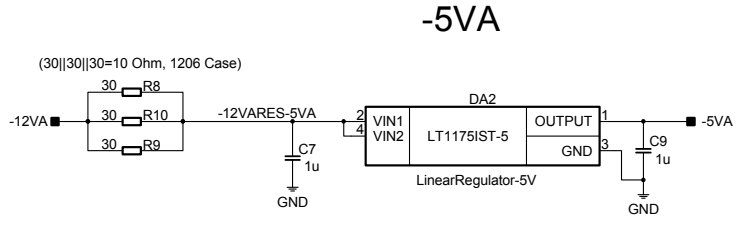


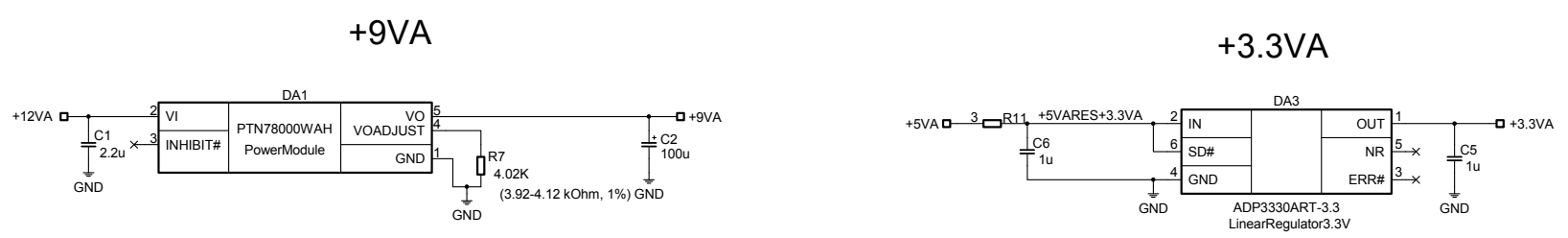
RF Blocks SPI Interfaces



Reference Clock Comparator Power Supply



RF Blocks Auxiliary Power Supply



Ф
E
D
C
B
A

Перв. примен.
FXPUP1-00M-PCB

Подл. и дата

Инд. № дубл.

Взам. инв. №

Подл. и дата

Инв. № подл.

HeadURL: <https://hyper.advantex.ru/svn/fxpupi/trunk/PCB/FXPUP1-B/BorderData.asc>

Изм/Лист	№ докум.	Подп.	Дата
Разраб.	Поляков		23.06.2008
Пров.	Бобкович		
Т. контр	Голубинский		
Н. контр			
Утв.	Поляков		

FXPUP1-B-01M-PCB ЭЗ
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Арт.	Масса	Масштаб
.	.	1:4

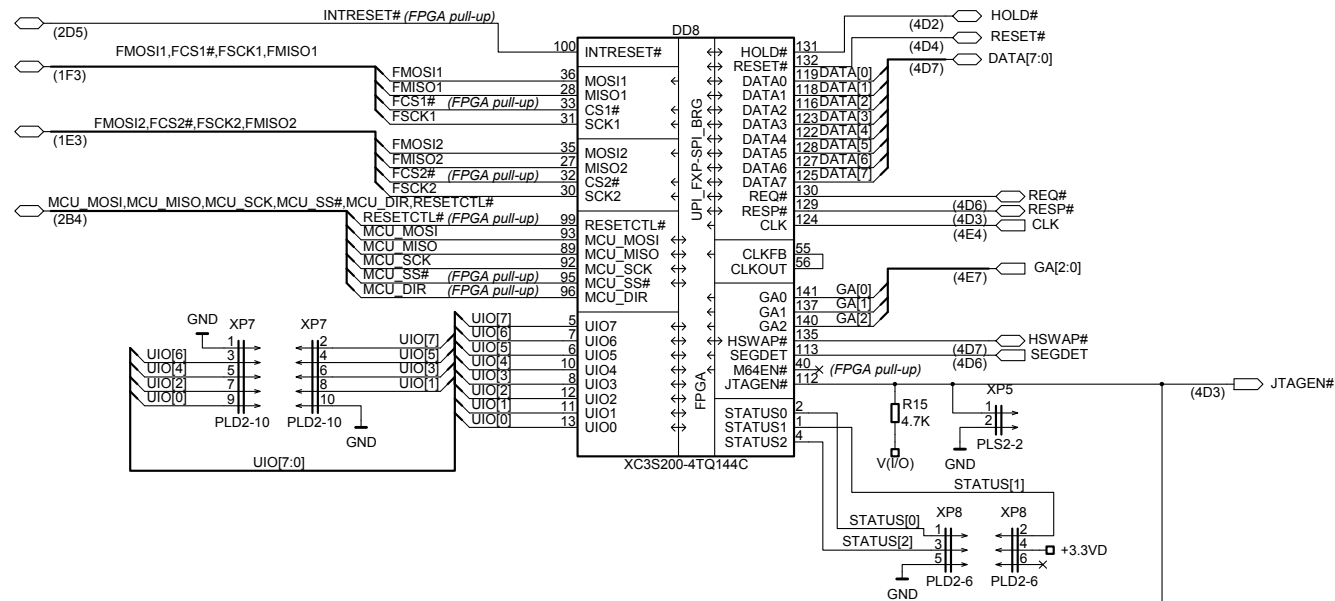
Схема электрическая принципиальная

Лист	01	Листов	05
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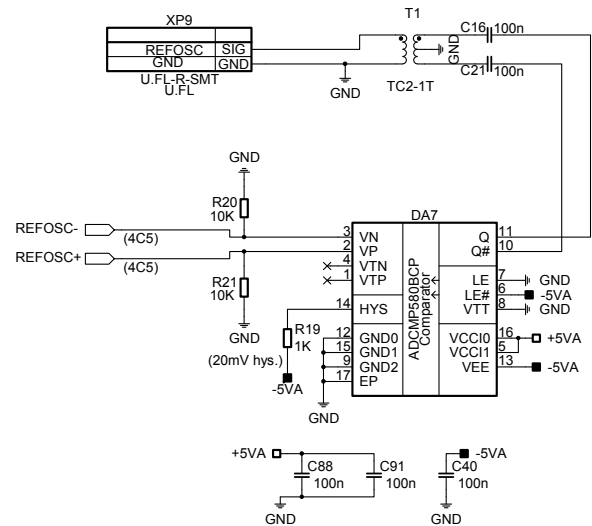
FR-4

ООО "Адвантех"
(Advantex LLC)

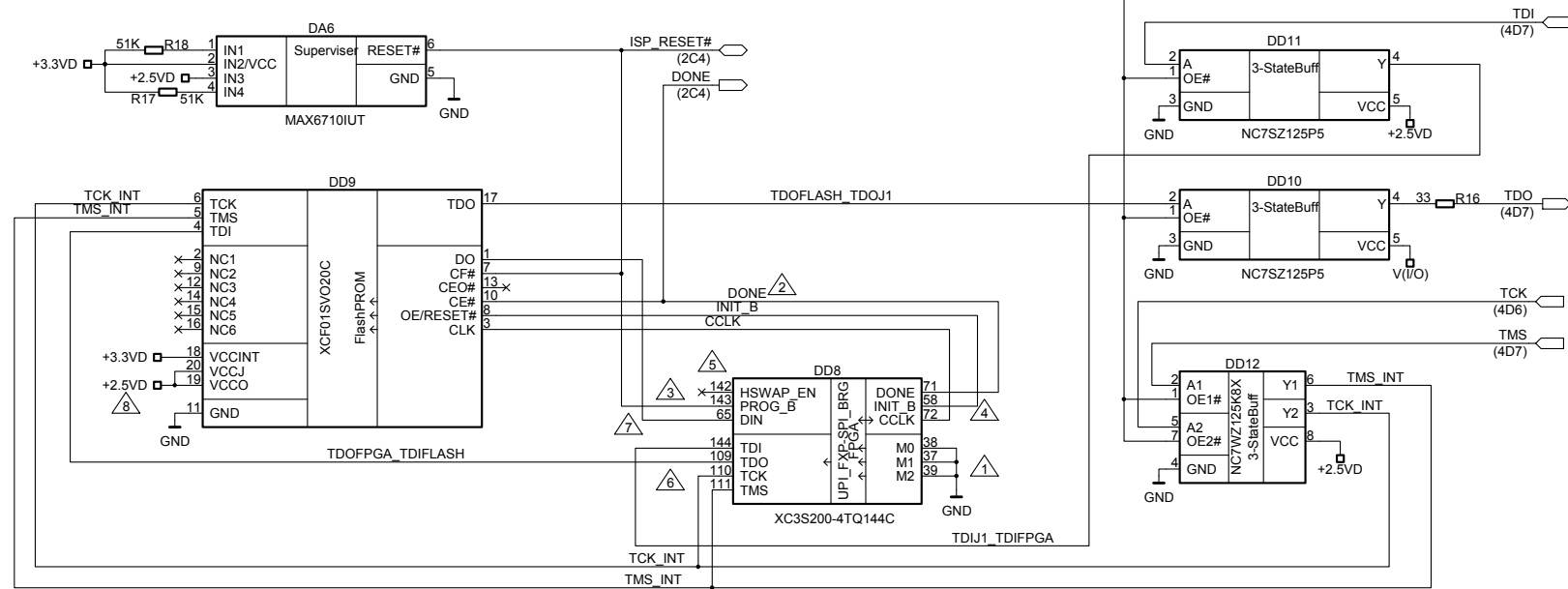
FPGA FXP to SPI Bridge



Backplane Reference Frequency



Configuration & JTAG



Notes:

- 1) Set Pull-down for M[2:0] pins in bitstream options to minimize power consumption via +2.5VD (Vccaux) after configuration
- 2) Set Drive or Pull-up bitstream option for DONE pin
- 3) Set ProgPin option to Pull-up after conf. (int. pulled-up to Vccaux during configuration)
- 4) Int. pulled-up during configuration. Set Persist:yes option to reserve the pin after configuration. If not it becomes user I/O pin. The pin has VCCO_4 or VCCO_BOTTOM power supply.
- 5) Int. pulled-up during configuration; defined by HswapenPin BitGen option after configuration.
- 6) All JTAG pins have int. pull-ups during configuration; defined by BitGen options after (should be pulled-up).
- 7) DIN pin has VCCO_4 supply rail.
- 8) Flash VCCO pin and FPGA VCCO_4 must have the same power supply voltage

FPGA Power Supply

